CLAIMS

1. Apparatus for frequency and phase locking a clock signal to an incoming video signal, comprising:

a system clock for generating a clock signal for frequency and phase locking to the incoming video signal;

a digitizer for digitizing the incoming video signal to yield a digitized color sub-carrier burst component;

a numerically controlled oscillator clocked by the system clock for generating a phase lock signal for locking to the incoming video signal;

a logic unit for sensing a static phase offset magnitude from an ideal 90° phase offset between the digitized color sub-carrier burst component and the numerically controlled oscillator output signal and for generating a compensating offset in accordance with the static phase offset signal for input to the system clock to drive the static offset to zero; and .

a color frame logic circuit for detecting phase alignment between a sync edge and the color sub-carrier burst component for determining the composite video input color frame sequence and for generating at least one pulse for resetting the numerically controlled oscillator.

2. The apparatus according to claim 1 wherein the numerically controlled oscillator further comprises a two-stage ratio counter for generating a multi-bit sub-carrier sinusoid having a prescribed frequency relationship with clock signal of the system clock.

3. The apparatus according to claim 1 wherein the system clock further comprises a voltage controlled oscillator that generates a 27 MHz clock signal.

4. The apparatus according to claim 3 wherein the numerically controlled oscillator further comprises a two-stage ratio counter for generating a multi-bit sub-carrier sinusoid having a prescribed frequency relationship with 27 MHz clock signal of the system clock such that sub-carrier/clock frequency ratio for an NTSC signal is 35/264, and 709379/4320000 a PAL signal.

5. The apparatus according to claim 1 wherein the logic unit further comprises:

a phase detector for detecting the phase difference between the digitized color sub-carrier burst component and the numerically controlled oscillator output signal and for generating an output signal which varies accordingly;

a phase lock detector responsive to the phase detector for generating an output flag once the numerically controlled oscillator output signal becomes phase locked to the digitized color-sub-carrier burst component; and

a static phase nulling circuit responsive to the phase detector output signal for generating a nulling signal for controlling the system clock to null the phase difference until receipt of the phase detector output flag.

6. The apparatus according to claim 1 wherein the digitizer comprises:

an analog to digital (A/D) converter for generating a digital output signal in accordance with the incoming video signal received at the input to the A/D converter;

a complimentary bandsplit filter for separating the color sub-carrier burst component from the digital input signal received from the A/D converter; and

a clamp for limiting the color sub-carrier burst component.

7. The apparatus according to claim 1 wherein the color frame logic circuit marks the beginning of the color frame sequence with a color frame pulse.

8. The apparatus according to claim 1 further including a counter block for counting pixels, lines and color frames to control a transition among normal operating mode at which the system clock signal is frequency and phase locked to the incoming video signal, a flywheel mode at which temporary losses of the incoming video signal are ignored and the system clock is held at a last correction mode, and free-running operation at which the system clock is forced to a calibrated value.

9. The apparatus according to claim 8 wherein the counter block further comprises:

a digital sync discriminator for generating a digital horizontal sync pulse in accordance with a horizontal sync pulse in the incoming video signal when the video signal is present;

a pixel counter responsive to the digital horizontal sync pulse for counting pixels; and

a state machine for controlling the pixel counter and for initiating the transition among normal, flywheel and free-running operation.

10. The apparatus according to claim 9 wherein the counter block further comprises:
a line counter for counting lines within the incoming video signal; an
a line counter state machine for controlling the operation of the line counter.

11. The apparatus according to claim 9 wherein the counter block further comprises:
a frame counter for counting frames within the incoming video signal; and
a frame counter state machine for controlling the operation of the frame counter.

12. A method for frequency and phase locking a clock signal to an incoming video signal, comprising the steps of :
generating a system clock signal for frequency and phase locking to the incoming video signal;
digitizing the incoming video signal to yield a digitized color sub-carrier burst component;
generating a phase lock signal for locking to the incoming video signal; and
sensing a static phase offset magnitude from an ideal 90° phase offset between the digitized color sub-carrier burst component and the phase lock signal; and
generating a compensating offset in accordance with the static phase offset signal for input to the system clock to drive the static offset to zero.

13. The method according to claim 12 wherein the step of generating a phase lock signal further comprises the step of generating a multi-bit sub-carrier sinusoid having a prescribed frequency relationship with the system clock signal.

14. The method according to claim 12 wherein the step of generating the system clock signal further comprises the step of generating a 27 MHz signal.

15. The method according to claim 14 wherein the step of generating the phase lock signal comprises the step of generating a multi-bit sub-carrier sinusoid having a prescribed frequency relationship with 27 MHz clock signal of the system clock such that sub-carrier/clock frequency ratio for an NTSC signal is 35/264, and 709379/4320000 a PAL signal.

16. The method according to claim 12 wherein the step of digitizing the incoming video signal further comprises the steps of:

converting the incoming video signal into a digital signal;

filtering the digital signal to separating the color sub-carrier burst component; and

limiting the color sub-carrier burst component.

17. The method according to claim 16 further including the step of detecting phase alignment between a sync edge and the color sub-carrier burst component for generating at least one pulse for resetting the numerically controlled oscillator and to determine a color frame sequence.

18. The method according to claim 1 further including the step of counting pixels, lines and color frames to control a transition among normal operating mode at which the system clock signal is frequency and phase locked to the incoming video signal, a flywheel mode at which temporary losses of the incoming video signal are ignored and the system clock is held at a last correction mode, and free-running operation at which the system clock is forced to a calibrated value.

19. Apparatus for frequency and phase locking a clock signal to an incoming video signal, comprising:

a system clock for generating a clock signal for frequency and phase locking to the incoming video signal;

a digitizer for digitizing the incoming video signal to yield a digitized color sub-carrier burst component;

a numerically controlled oscillator clocked by the system clock for generating a phase lock signal for locking to the incoming video signal; and

a logic unit for sensing a static phase offset magnitude from an ideal 90° phase offset between the digitized color sub-carrier burst component and the numerically controlled oscillator output signal and for generating a compensating offset in accordance with the static phase offset signal for input to the system clock to drive the static offset to zero; and

a counter block for counting pixels, lines and color frames in the incoming video signal to control a transition among normal operating mode at which the system clock signal is frequency and phase locked to the incoming video signal, a flywheel mode at which temporary losses of the

incoming video signal are ignored and the system clock is held at a last correction mode, and free-running operation at which the system clock is forced to a calibrated value.

20. The apparatus according to claim 19 wherein the counter block further comprises:

a digital sync discriminator for generating a digital horizontal sync pulse in accordance with a horizontal sync pulse in the incoming video signal when the video signal is present;

a pixel counter responsive to the digital horizontal sync pulse for counting pixels; and

a state machine for controlling the pixel counter and for initiating the transition among normal, flywheel and free-running operation.

21. The apparatus according to claim 19 wherein the counter block further comprises:

a line counter for counting lines within the incoming video signal; an

a line counter state machine for controlling the operation of the line counter.

22. The apparatus according to claim 19 wherein the counter block further comprises:

a frame counter for counting frames within the incoming video signal; and

a frame counter state machine for controlling the operation of the frame counter.